IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each semiconductor substrate element of said substrate elements including integrated circuitry, comprising:

providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side in a first wafer having a periphery having a portion thereof including a flat;

providing a second semiconductor substrate element having a first side including integrated circuitry thereon and having a backside in a second wafer having a periphery having a portion thereof including a flat;

stacking said first semiconductor substrate element and ~~said~~ the [at least one] second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the second semiconductor substrate element having the periphery of said first semiconductor substrate element substantially aligned with the periphery of said second semiconductor substrate element, said first semiconductor substrate element and the second semiconductor substrate element for locating a portion of the integrated circuitry on said first semiconductor substrate element vertically spaced from [adjacent] a portion of the integrated circuitry on the second semiconductor substrate element for vertical alignment of said first semiconductor element and said second semiconductor substrate element; and

severing from said stack traversely at least one dice pair comprising a die from said first semiconductor substrate element and a second die from said [at least one] second semiconductor substrate element; and

adhesively attaching said first semiconductor substrate element and said [at least one] second semiconductor substrate element.

2. (Original) The method of claim 1, wherein said adhesive comprises a dielectric adhesive.

3. (Amended) The method of claim 1, further including:
disposing a heat sink element between said first semiconductor substrate element and said [at least one] second semiconductor substrate element.

4. (Previously Twice Amended) The method of claim 1, wherein said first semiconductor substrate element and the second semiconductor substrate element, each semiconductor substrate element of the first semiconductor element and the second semiconductor element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. (Currently Amended) The method of claim 1, wherein said first semiconductor substrate element and said [at least one] second semiconductor substrate element each include a flat, and ~~said~~ a vertical alignment is effected by aligning said flat of said first semiconductor substrate element and said flat of the [at least one] second semiconductor substrate element by stacking said first semiconductor element and the second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the second semiconductor substrate element having the periphery of said first semiconductor substrate element substantially aligned with the periphery of said second semiconductor substrate element, said first semiconductor substrate element and the second semiconductor substrate element for locating a portion of the integrated circuitry on said first semiconductor substrate element vertically spaced from a portion of the integrated circuitry on the second semiconductor substrate element.

6. (Previously Amended) The method of claim 1, further comprising:
connecting a first die of said at least one dice pair to [conductors of] a substrate having conductors.

7. (Original) The method of claim 6, wherein said connection is selected from a group comprising reflowable metal elements, polymer elements having a conductive capability, and preformed lead-type elements.

8. (Amended) The method of claim 6, further comprising:
connecting both dice of said at least one dice pair to said conductors of said substrate.

9. (Original) The method of claim 6, further comprising:
connecting the second die of said at least one dice pair to portions of the conductors of said substrate through intermediate connection elements.

10. (Previously Amended) The method of claim 9, wherein said intermediate connection elements are selected from a group consisting of bond wires and traces of flex circuits.

11. (Previously Twice Amended) The method of claim 10, further comprising:
connecting said at least one dice pair to portions of the conductors of said substrate and encapsulating said at least one dice pair thereafter.